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RE: Docket No. RCA 88228

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Kranawetter et al.	Art Unit: 2613	
Serial No.:	09/319,324	Examiner: Behrooz M. Senfi	
Filed:	June 3, 1999		
Title:	PARALLEL DECODING OF INTERLEAVED DATA STREAMS WITHIN AN MPEG DECODER		

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APPLICANTS' REPLY BRIEF

For the reasons set forth below, Applicant respectfully requests that this REPLY BRIEF be considered by the Board in connection with the Appeal of the Examiner's Final Rejection dated October 2, 2003.

NEW ISSUES RAISED IN EXAMINER'S ANSWER

In the Examiner's Answer (see Page 7), reference is made for the first time to Figure 6 of the previously cited Park et al Patent No. 5,675,424. This figure has not previously been the basis of any rejection and therefore it, along with the Examiner's characterization of that figure, require explanation and further consideration.

ISSUES

As stated in Applicants' Brief on Appeal, there is only one principal issue in this case– does Park disclose or suggest anything "for producing decoded image information selectable for

producing either high resolution or reduced data image reproduction of a complete image" (claim 1 or the similar language at the end of claims 7 and 13) as required by each of Appellant's rejected claims ?

The Examiner has newly relied upon Fig. 6 of the previously cited Park patent for a purported showing of the above-quoted requirement of each of the claims on appeal.

A secondary issue for the Board is whether there is any suggestion or motivation in either cited reference to combine them and/or to modify either or both references in any manner to arrive at the combinations set forth in the rejected claims.

GROUPING OF CLAIMS

Claims 1 – 6 stand as one group (apparatus claims), claims 7 – 12 stand as a second group (first method claims) and claims 13 – 15 stand as a third group (second method claims).

ARGUMENT

Rejection of Apparatus Claims 1 – 7 Under 35 U.S.C. 103(a)

With respect to the rejection of claims 1 – 6, (particularly independent claim 1), the Examiner has not indicated any embodiment in the cited references which meets the language "for producing decoded image information selectable for producing either high resolution or reduced data image reproduction of a complete image" (claim 1). To fill this gap, the Examiner stated at the end of the Final Rejection of claim 1, apparently with respect to Park:

"(whole purpose of dividing the bit stream to multiple bit streams and processing through multiple encoders and decoders are to make the signal selectable/suitable for high/low resolution based on the desired application)".

The Examiner's conclusion is not supported. Neither Park nor Yoon says any such thing and neither says anything about making a signal "selectable/suitable for high/low

resolution based on the desired application". That statement is solely attributable to the Examiner and not to either cited reference.

In actual fact, the "whole purpose" of Park in "dividing the bit stream to multiple bit streams" according to Park is to be able to process several image bit streams in parallel "using a reduced clock frequency fs/4" (col. 2, lines 45 – 48; col.3. lines 17 – 18; col. 4, lines 6 – 9 and lines 21 – 22; see also col. 5, lines 12 – 17 for use of a reduced frequency fs/2).

Park's Fig. 4 embodiment uses four parallel image signal processing channels, each operating at fs/4, while the included motion compensation processor operates at fs (col. 4, lines 5 – 12, lines 27 – 33). In Park's (newly cited) Fig. 6 embodiment, a different configuration is shown for handling a different signal format in which only two parallel image signal processing channels are used, each operating at fs/2, while the corresponding motion compensation processor would operate at fs (col. 5, lines 12 – 24).

Neither the Fig. 4 embodiment nor the DIFFERENT Fig. 6 embodiment of Park discloses anything about a single configuration including apparatus "for producing decoded image information selectable for producing either high resolution or reduced data image reproduction of a complete image" (emphasis added).. There is just nothing "selectable'" for producing any "either" "or" in any of Park's configurations.

It should be noted that the Examiner previously relied principally on Figs. 3A – 3B of Park. Figs. 1, 2, 3A and 3B of Park are described in Columns 1 and 2 under the heading "Description of the Prior Art" and are referred to as "conventional" in the description. Those figures are therefore clearly not part of Park's invention and, in fact, Park goes to some lengths to differentiate his claimed configurations (Figs. 4 and 6) from the prior art configurations of Figs. 1 – 3B. Nevertheless, the Examiner, as he has throughout this application process, now

relies upon elements from Fig. 3B in combination with Figs 4 and 6, along with elements from the secondary reference, Yoon.

As described by Park, the prior art system uses a technique of "slicing" the overall image into horizontal, multi-line "subpictures" P1 - Pn (see Park, FIG.2) and processing each of those slices in a separate decoder.

In the "Background of Invention" portion of Park, referring to the "Prior Art" shown in FIGS. 1 – 3B, Park states:

"conventional image encoder section and decoder section (which) apply a parallel processing method with division of picture", i.e. "one frame image is divided into subpictures P1 through Pn and image data on respective subpictures are parallel-signal processed by encoders (or decoders) operated individually, and the signal process for the overall frame is completed by summing the outputs of the respective encoders",

all of which is undertaken

"to process a video signal with a clock signal having a relatively lower frequency" (col. 1, lines 43 – 52).

Thus, Park describes the objective of the prior art system as follows (Park, col. 1, lines 43 – 46):

> "The conventional image encoder section and decoder section apply a parallel processing method with division of picture to process a video signal <u>with a clock signal having a relatively lower frequency"</u>
>
> (emphasis added)

Park is referring to a "relatively lower frequency" as compared to the clock frequency of 75 MHz used to digitize the original HDTV signal. Park goes on to say "the signal process for the

overall frame is completed by summing the outputs of the respective encoders." (col. 1, lines 51 – 53).

There is no mention whatsoever of " producing decoded image information selectable for producing either high resolution or reduced data image reproduction of a complete image" as required by claims 1 – 6.

Park's invention is directed to combining a lower frequency encoder/decoder sampling clock system with a higher frequency sampling clock for motion compensation elements, such as are found in MPEG and HDTV signal formats (see col. 2, lines 45 – 51).

In view of the confusing manner in which the Examiner's position is expressed in the Answer, and the fact that much of what is said is not found in Park, the first portion of the Examiner's argument is set out verbatim :

> "Park '424 reference is related to an image decoding for an image compression/expansion system of HDTV (which is considered as an high resolution) and/or MPEG standard (which is considered as lower or reduced resolution) for reproducing the complete image, in particular (i.e. fig. 6, col. 5, lines 12 -24) teaches that the present (sic) invention can select/applied to MPEG standard having lower reduce resolution than HDTV."

It will be assumed that the reference to "the present invention" refers to Park. In fact, Park discloses two separate embodiments of his claimed configuration, one in Fig. 4 and a different one in Fig. 6. As noted above, the Fig. 6 embodiment is relied upon by the Examiner for the first time in the Answer.

The Examiner has missed or misunderstood an important point.

While Park refers to HDTV (referred to by the Examiner as "high resolution") image signals in connection with his Fig. 4 embodiment, and to MPEG (characterized by the Examiner as "lower resolution" images) in connection with his Fig. 6 embodiment, in each

case, if it is high resolution "in", it is high resolution "out" (Fig. 4) and, if it is low resolution "in", it is low resolution "out" (Fig. 6).

Nowhere does Park say (or does the Examiner point out) anything about a single embodiment (as presently claimed) in which there is "a data stream of MPEG coded data" from which "first and second datastreams" are derived, the first datastream being constituted by --- interleaved first and second spatially adjacent pixel block components and said second datastream being constituted by ---- interleaved third and fourth ---spatially adjacent pixel block components", with the result (not ever suggested or disclosed by Park or Yoon) of "producing decoded image information selectable for producing either high resolution or reduced data image reproduction of a complete image" (claim 1, emphasis added).

Yoon is relied upon by the Examiner for disclosing spatially adjacent pixel block components. However, no relationship is established by the Examiner between Yoon and Park It is respectfully submitted that these references are not combinable (no suggestion or disclosure to support the combination) and therefore, there is no suitable basis for the obviousness rejection based on any combination of Yoon and Park.

Each of claims 1 – 6 therefore is clearly patentable over the cited art and should be allowed.

Rejection of Claims 7 – 12 Under 35 U.S.C. 103(a)

With respect to method claims.7 – 12, independent claim 7 requires:

"said producing step comprises producing multiple datastreams, each datastream having a different predetermined sequence of mutually interleaved pixel block components selectable for either high resolution or reduced resolution data image reproduction modes for a complete image".

The "prior art" disclosure in Park on which the Examiner has relied neither discloses nor suggests any such datastreams which are "selectable for either high resolution or reduced resolution, etc." as pointed out above.

Yoon is silent on this aspect of the claimed method.

Each of method claims 7 – 12 is therefore submitted to be patentable over the cited art.

Rejection of Claims 13 – 15 Under 35 U.S.C. 103(a)

With respect to method claims 13 – 15, independent claim 13 requires:

"decoding said first and second datastreams to produce decoded image information selectable for reproducing complete images in either high resolution or reduced resolution image reproduction modes."

The "prior art" disclosure in Park on which the Examiner has relied neither discloses nor suggests "decoding" any such datastreams "to produce decoded image information selectable for reproducing complete images in either high resolution or reduced resolution, etc." as pointed out above.

Yoon is silent on this aspect of the claimed method.

Each of method claims 13 – 15 is therefore submitted to be patentable over the cited art.

COMBINATION OF REFERENCES

The Examiner cited Yoon '135 in the Final Rejection since "Park '424 fails to explicitly teach the newly added limitation "spatially adjacent pixel"". It is recognized that Yoon discloses "carrying out a parallel processing by dividing a macro block into four subblocks" (col. 2, lines 46 – 48). However, Yoon does not mention first and second datastreams , each with two interleaved spatially adjacent pixel block components as recited in the rejected claims. In addition, Yoon is silent, as noted above, regarding the other specific elements recited in each of the claims on appeal. As such, it is respectfully submitted that there is no basis for combining Yoon with Park to support a rejection of such claims.

CONCLUSION

The cited prior art is totally lacking in any disclosure or mention of an element of each of the rejected claims. There is no basis for concluding that such claims are unpatentable under 35 USC 103 (a).

In view of the foregoing, reversal of the Examiner's rejection and allowance of claims 1 - 15 are respectfully requested.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this amendment is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to the Commissioner for Patents; P.O. Box 1450; Alexandria, VA 22313-1450 on:

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APPENDIX

CLAIMS

Claim 1 An MPEG compatible digital signal processing system comprising:

an input network for receiving a data stream of MPEG coded data;

a coupling network responsive to said datastream for deriving therefrom a predetermined sequence of image data; and

an image signal processor responsive to said image data wherein

said coupling network comprises interleaving means responsive to said datastream of MPEG coded data for deriving therefrom at least first and second datastreams, said first datastream being constituted by a first predetermined sequence of interleaved first and second spatially adjacent pixel block components and said second datastream being constituted by a second predetermined sequence of interleaved third and fourth spatially adjacent pixel block components for producing decoded image information selectable for producing either high resolution or reduced data image reproduction of a complete image.

Claim 2 A system according to claim 1, wherein

said interleaved image data comprises data block components of an MPEG compatible macroblock containing pixel representative information.

Claim 3 A system according to claim 1, wherein:

said interleaving means produces a first datastream of interleaved first and second spatially adjacent pixel block components from each macroblock of said MPEG coded data and a second datastream of interleaved third and fourth spatially adjacent pixel block components from each macroblock of said MPEG coded data.

Claim 4 A system according to claim 3, wherein

Said first, second, third and fourth pixel block components are spatially adjacent components of an MPEG compatible macroblock.

Claim 5 A system according to claim 1, wherein said input network includes

a decoder for decoding said MPEG coded datastream; and

a decompressor for decompressing output signals from said decoder; wherein

said interleaving network responds to output signals from said decompressor.

Claim 6 A system according to claim 1 and further including

a memory for storing image representative data; and

a motion compensation network coupled to said memory; wherein

said image signal processor and said motion compensation network comprise a DPCM loop.

Claim 7 A method for processing a datastream of MPEG coded image representative data, comprising the steps of:

decoding said data to produce a decoded datastream;

producing from said decoded datastream a predetermined sequence of interleaved data blocks representing image pixels;

processing said data blocks; and

storing data blocks from said processing step; wherein

said producing step comprises producing multiple datastreams, each datastream having a different predetermined sequence of mutually interleaved pixel block components suitable selectable for either high resolution or reduced resolution data image reproduction modes for a complete image.

Claim 8 A method according to claim 7, wherein

said producing step produces a first datastream of interleaved spatially adjacent first and second pixel block components, and a second datastream of interleaved spatially adjacent third and fourth pixel block components.

Claim 9 A method according to claim 8, wherein

said interleaved pixel blocks comprise an MPEG compatible macroblock.

Claim 10 A method according to claim 7, wherein

said processing step includes DPCM processing of pixel data.

Claim 11 A method according to claim 10, wherein said DPCM processing step includes the further steps of

decompressing data blocks stored in said storing step; and

motion compensation processing decompressed data blocks produced by said decompressing step.

Claim 12 A method according to claim 9, wherein

said processing step comprises the steps of predicting pixel values and compressing pixel values.

Claim 13 A method for processing a datastream of MPEG coded image representative data, comprising the steps of:

receiving an input datastream of MPEG coded data;

decoding said input datastream to produce a decoded datastream of data blocks containing pixel representative information;

processing said decoded datastream of datablocks to produce therefrom a first datastream comprising at least first and second groups of data block components having pixel representative information interleaved in a first predetermined sequence, and a second datastream comprising at least third and fourth groups of data block components having pixel representative information interleaved in a second predetermined sequence; and

decoding said first and second datastreams to produce decoded image information selectable for reproducing complete images in either high resolution or reduced resolution image reprduction modes.

Claim 14 A method according to claim 13, wherein

said first group is constituted by first and second pixel blocks of an MPEG compatible macroblock; and

said second group is constituted by third and fourth pixel blocks of an MPEG compatible macroblock.

Claim 15 A method according to claim 14, wherein

said first, second, third and fourth groups comprise the same macroblock.